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On the some electrical properties of the non-ideal PPy/p-Si/Al structure

Ş. Aydoğan*, M. Sağlam, A. Türüt

Department of Physics, Faculty of Sciences and Arts, University of Atatürk, 25240 Erzurum, Turkey

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Abstract

The electrical analysis of the PPy/p-Si structure has been investigated by means of *I–V, C–V* and *C–f* measurements. The diode ideality factor and the barrier height have been obtained to be $n=1.78$ and $\Phi_b=0.69$ eV by applying a thermionic emission theory, respectively. At high current densities in the forward direction, the series resistance effect has been observed. In general, the barrier height obtained from *C–V* data is greater than obtained from the *I–V*. This has been explained by introducing a spatial distribution of barrier heights (BHs) due to barrier height inhomogeneities that present at the PPy/p-Si interface. The *C–f* measurements of the structure have been performed at various biases and it has been seen that they have a good agreement between experimental and theoretical values. The interface state density N_{ss} and relaxation time τ of the structure have been determined from the *C–f* characteristics.
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Keywords: Polypyrrole; Ideality factor; Barrier height

1. Introduction

Polymer electronics has attracted considerably interest in the recent years with the discovery of conducting polymers, which could be used as active components in electronic devices. Among the conjugated conducting polymers, polyaniline (PANI) and polypyrrole (PPy) have attracted much interest worldwide because of their high environmental, thermal and chemical stability and their high conductivities. The electrical conductivity of these polymers is between 10^{-5} and 10^{2} S/cm while being doped, whereas common insulators exhibit conductivities below 10^{-12} S/cm [1–3]. Conducting polymers are expected to yield numerous potential applications such as biosensors, electrochemical sensors, polymeric voltaic cell, electroluminescent devices, field effect transistor, light emitting diodes, capacitors and Schottky diodes have been fabricated and tested by using conducting polymers [4–6]. Rectifying junctions are the basic elements of many electronic components. Since the discovery of the conducting polymers, rectifying junctions such as p–n junction and Schottky junction have been studied so as to explore the possible application of conducting polymers.

In a Schottky diode (or rectifying contacts) some parameters, such as ideality factor, barrier height and series resistance effect, the performance of the device. These parameters give useful information concerned with the nature of the diode. The classical model of a Schottky diode assumes the junction to be abrupt with a fixed barrier height.

The electrochemical polymerization method is one of the simplest and most convenient methods of preparation of thin films for various devices. The thickness and the area of the film are easily controlled by this method. Furthermore, conducting polymers are easily doped and undoped by an electrochemical method, by controlling the polarity and current. The importance of the present study is that the polymer is directly formed by an anodization method under constant current density condition on a p-type Si substrate. The main goal of this paper is the calculation of the characteristic parameters such as ideality factor, barrier height, and series resistance, density of interface states (at the interface) of the polypyrrole/p-Si obtained from current–voltage (*I–V*), capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) characteristics at room temperature in dark.

2. Experimental procedure

p-type Si semiconductor wafer with (100) orientation and 400 μm thickness and 1–10 Ω cm resistivity was used before making contacts, the wafer was chemically cleaned using the RCA cleaning procedure (i.e. 10 min boil in $NH_3+H_2O_2+$

* Corresponding author.
E-mail address: saydogan@atauni.edu.tr (Ş. Aydoğan), saydogan43@yahoo.com (Ş. Aydoğan).

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$6H_2O$ followed by a 10 min $HCl+H_2O_2+6H_2O$ at 60 °C). The ohmic contact was made by evaporating Al on the back of the p-Si substrate, then was annealed at 580 °C for 3 min in N_2 atmosphere. The native oxide on the front surface of substrate was removed in $HF+10H_2O$ solution. Finally, it was rinsed in de-ionised water for 30 s and was dried. The edges of semiconductor used as an anode were covered by wax so that the polished and cleaned front side of sample (with circular area of 1.7 mm diameter) was exposed to the electrolyte by mounting it in an experimental set-up employed for anodization. The electrolyte solution which was composed of 0.4 M pyrrole and 0.1 M tetrabutylammonium tetrafluoroborate was prepared in a propylene carbonate solvent (Merck trademark). A platinum plate was used as a cathode. The polymer film was electrochemically deposited (the anodization method) on the surface of p-type Si semiconductor in electrolyte solution under the condition of constant temperature of 45 °C and a constant current density of 4 mA/cm^2. After polymerization process was carried out, the surface coated polypyrrole was cleaned by acetonitrile for 10 min at room temperature and was dried. In this way, the PPy/p-Si/Al structure was obtained. The thickness of PPy layer was calculated as 210 nm approximately from high frequency C–V measurements by using $C=\varepsilon\varepsilon_0/d$ equation. The I–V measurements of this structure were performed using KEITLEY 487 Picoammeter/Voltage Source, the C–V and C–f measurements were performed with HP 4192A, (50 Hz to 13 MHz) LF impedence analyzer at room temperature in dark.

3. Results and discussion

As is indicated above, the conducting polymers are easily doped and undoped by an electrochemical method. It is well known that changing the oxidation level of a conjugated polymer means changing the number of electrons on its backbone. Oxidation means removing electrons, reduction adding electrons. This process can be done electrochemically, and the potential difference between oxidized and reduced states is usually less than 1 V. The oxidation level varies continuously and smoothly between the fully oxidized and fully reduced states and can be held at any state by the appropriate potential. As has been given in [8], Fig. 1 is a schematic illustration of the oxidation process in polypyrrole, going from the neutral, insulating state (top) to a partially oxidized state (middle) to the fully oxidized conducting state (bottom). To maintain charge neutrality, an anion is inserted into the material for each positive charge on the chain [8].

According to the thermoionic emission (TE) theory, the current in Schottky barrier diodes (SBDs) can be expressed as [7]:

$$I = AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \quad (1)$$

where

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right) \quad (2)$$

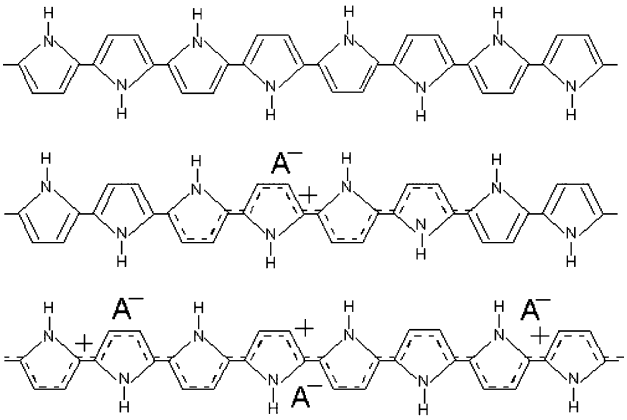

Fig. 1. A schematic illustration of the oxidation process in polypyrrole.

is the saturation current, Φ_b is the effective barrier height at zero bias, A^* is the Richardson constant and equals to 32 A/cm^2 K^2 for p-type Si [9–11], where q is the electron charge, V is the forward-bias voltage, A, is the effective diode area, k is the Boltzmann's constant, T is the temperature in Kelvin, n is the ideality factor, and it is determined from the slope of the linear region of the forward bias $\ln I$–V characteristics through the relation:

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

$n=1$ for an ideal diode. However, n has usually a value greater than unity. High values of n can be attributed to the presence of the interfacial thin native oxide layer and a wide distribution of low-SBH patches (or barrier inhomogeneities), and, therefore, to the bias voltage dependence of the SBH [9–11]. On the other hand, the barrier height can be obtained from the equation,

$$q\Phi_b = kT\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

Fig. 2 presents the forward bias current–voltage (I–V) characteristics of the PPy/p-Si/Al structure. The values of the ideality factor and barrier height were found to be $n=1.78$ and $\Phi_b=0.69$ eV, respectively, by using Eqs. (3) and (4). It is seen that the structure is not an ideal contact. In real Schottky contacts, an ideal behaviour deviation is frequently observed and the I–V curves cannot be fit by Eq. (1). The Schottky effect, series resistance, leakage current, the presence of other transport mechanisms [7], the presence of a thin interface insulator layer, probably an native oxide layer, at the PPy and semiconductor interface due to p-Si is exposed to air before forming the PPy [12] and inhomogeneous Schottky barrier heights [13,14] can be the most important causes of non-ideal behaviour. But, we attributed this non-ideal behavior to effects of the bias voltage drop across the interfacial native oxide layer and series resistance, therefore, of the bias voltage dependence of the barrier height. The formation of such a thin interfacial layer is inevitable during the fabrication of the device by the

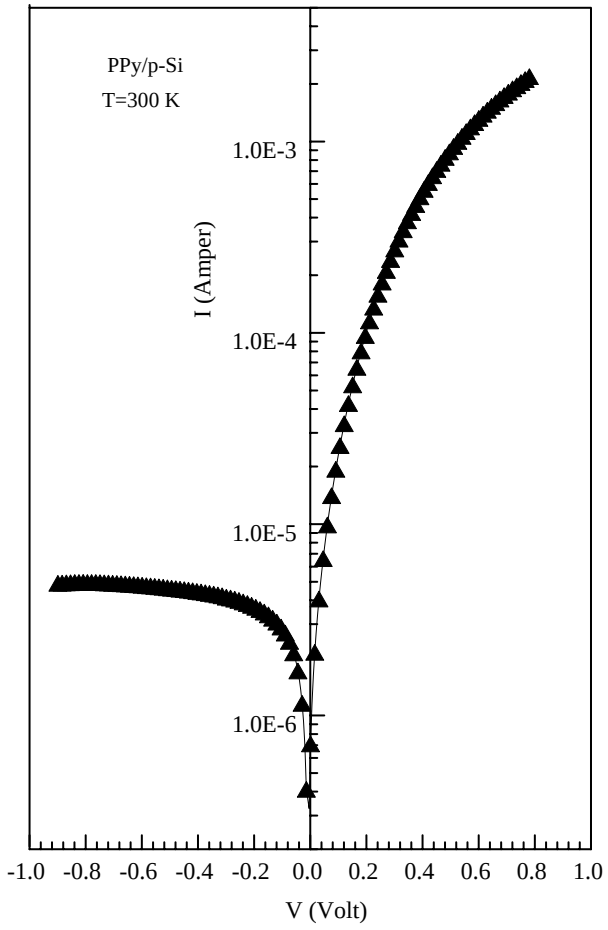

Fig. 2. The forward and reverse bias the current–voltage characteristics of the PPy/p-Si structure.

conventional techniques and before coating of PPy on the front surface of the semiconductor substrate [12].

On a semi-log scale and at low forward bias voltage, the forward bias *I–V* characteristics of the metal semiconductor contacts are linear but deviate considerably from linearity due to the some factors at large voltages. One of the factors is series resistance (R_s). When the applied voltage is sufficiently large, the effect of the R_s can be seen at the non-linear regions of the forward bias *I–V* characteristics. The lower the series resistance, the greater the range over which the *I–V* curve yields a straight line [15]. The values of the R_s were achieved using a method developed by Cheung and Cheung [16] in the high current range where the *I–V* characteristics are not linear. The forward bias *I–V* characteristics due to the TE of a Schottky diode with the series resistance can be expressed as:

$$I = I_0 \exp\left[\frac{q(V - IR_s)}{nkT}\right] \tag{5}$$

where the IR_s term is the voltage drop across series resistance of device. The values of the series resistance

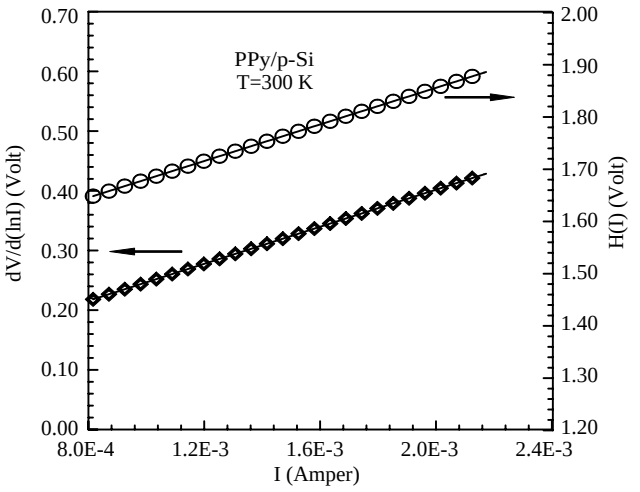

Fig. 3. A plot of d*V*/d(ln *I*) vs *I* and *H*(*I*) vs *I*, obtained from forward bias current–voltage characteristics of the PPy/p-Si structure.

can be determined from following functions, using Eq. (5).

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_s \tag{6}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{7}$$

and $H(I)$ is given as follows:

$$H(I) = n\Phi_b + IR_s \tag{8}$$

A plot of d*V*/d(ln *I*) vs *I* will be linear and give R_s as the slope and nkT/q as the *y*-axis intercept, from this the values of *n* will be determined from Eq. (6). Fig. 3 shows a plot of d*V*/d(ln *I*) and *H*(*I*) vs *I*. The parameters of the structure, *n*, Φ_b, R_s, obtained from both plots by using Eq. (6) as $n = 3.53$, $R_s = 155\ \Omega$ and by using Eq. (8) as $R_s = 165\ \Omega$, $\Phi_b = 0.64$ eV. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. However, it can be clearly seen that there is relatively a high difference between the values of the ideality factor obtained from the downward curvature regions of forward bias *I–V* plots and from the linear regions of the same characteristics. The reason for this difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the Schottky barrier height according to the voltage drop across the interfacial layer and change of the interface states with bias in this concave region of the *I–V* plot [7].

The *C–V* measurement is another method to determine the barrier height. It is convenient to examine capacitance–voltage (*C–V*) data for rectifying contacts by plotting $1/C^2$ vs voltage (*V*) for reverse bias. The capacitance is measured at different reverse bias values by superimposing an ac voltage on the dc voltage. When the dc voltage corresponds to a reverse bias, the differential capacitance represents the response of the depletion layer to the Ac signal. In simple Schottky barrier theory the capacitance of the barrier varies

with applied reverse voltage V in such a way that a straight line is obtained if $1/C^2$ is plotted against V. This relation is given by the expression;

$$C^{-2} = \frac{2(V_d + V)}{\varepsilon_s \varepsilon_0 q A^2 N_A} \tag{9}$$

where V_d is the diffusion potential at zero bias which is determined from the extrapolation of the linear $1/C^2$–V plot to the V axis, A is the effective area of the diode and ε_s is the dielectric constant of the semiconductor ($=11.7$ for Si), ε_0 is the dielectric constant of vacuum ($=8.85\times10^{-14}$ F/m) and N_A is the concentration of ionized acceptors and it is written as:

$$N_A = N_V \exp\left(\frac{V_p}{kT}\right) \tag{10}$$

The value of the barrier height Φ_b can be calculated by the following well-known equation, using C–V measurements,

$$\Phi_b = V_d + V_p \tag{11}$$

where V_p is the potential difference between the Fermi level and the top of the valence band in the neutral region of p-Si and can be calculated from the carrier concentration N_A; it is obtained from relation $V_p = kT\ln(N_v/N_A)$ where $N_v = 1.82\times10^{19}\,\mathrm{cm}^{-3}$ is the state density in the valence band.

Fig. 4 shows the reverse bias C–V characteristics of the structure at various frequencies. It can be seen from this figure that at low frequencies the values of capacitance are shown to increase. The dependence of the capacitance of a rectifying contact upon frequency can also arise due to the presence of deep lying impurities in the depletion region of semiconductor. Deep impurities are energy levels of intrinsic lattice defects or impurity atoms that have energy near the center of the band gap. Presence of deep traps in the depletion region of the Schottky barrier makes the junction capacitance a complicated function of the bias voltage and the measuring frequency. Also, it is observed that the low-frequency capacitance increases with the applied bias while the high-frequency capacitance remains almost constant. This observation may be attributed to the capacitive response of interface states to the measurement frequency. In general, at sufficiently high frequencies ($f \geq 500$ kHz) the interface states do not contribute to the capacitance [17]. Fig. 5 shows the reverse bias C^{-2}–V characteristics of the PPy/p-Si structure at various frequencies. The plots of $1/C^2$ as a function of reverse bias voltage are linear which indicates the formation of Schottky junction. As can be seen from Fig. 5, the slope of C^{-2}–V curves decrease with increasing frequency. This case can be explained by whether the interface state charges contribute to the diode capacitance or the charge at the interface states can follow an alternating-current signal. Usually, at the interfacial and layer semiconductor interface, there are various kinds of states with different lifetimes. At low frequencies, all the interface states affected by the applied signal are able to give up and accept charges in response to this signal. The interface state capacitance appears directly in parallel with the depletion capacitance, and this result in a higher total value of the capacitance for Schottky diodes than if no interface states were present. At intermediate frequencies, some, but not all, of the interface state charge will participate in small signal measurements, and values of the capacitance observed will be between the low- and high-frequency values. If the capacitance measurements are made at sufficiently high frequencies, the interface state charges do not contribute to the diode capacitance. This will occur when the time constant is too long to permit the charge to move in and out of the interface states in response to an applied signal [20].

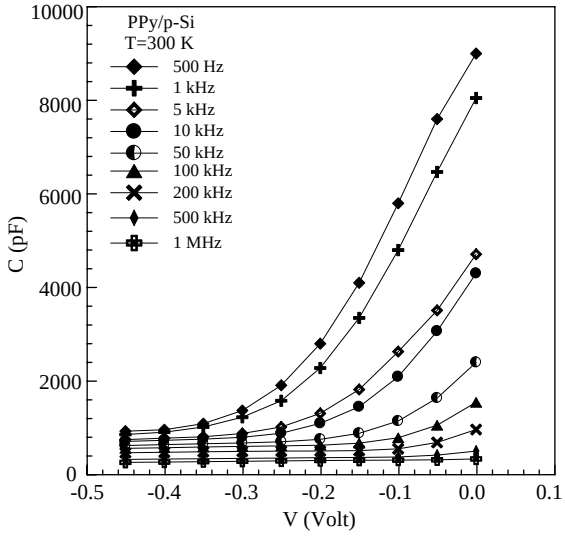

Fig. 4. The reverse bias C–V characteristics of the PPy/p-Si structure at various frequencies.

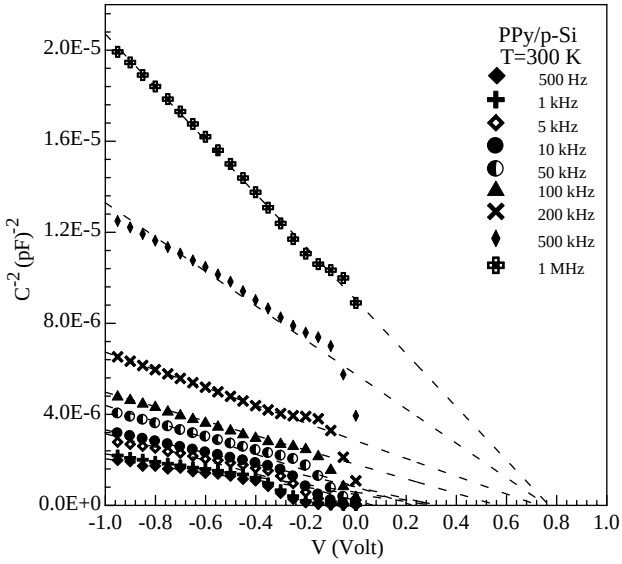

Fig. 5. The reverse-bias C^{-2}–V characteristics of the PPy/p-Si structure at various frequencies.

Table 1
Some parameters of the structure are given in the table by using the reverse bias *C–V* characteristics

$T=300$ K	PPy/p-Si								
f (kHz)	0.5	1	5	10	50	100	200	500	1000
V_d (eV)	0.31	0.34	0.34	0.30	0.35	0.56	0.73	0.76	0.77
N_a (cm^{-3})$\times 10^{16}$	1.50	1.38	1.29	0.93	0.65	0.73	0.60	0.31	0.20
V_p (eV)	0.170	0.171	0.173	0.181	0.191	0.188	0.193	0.210	0.162
Φ_b (V)	0.480	0.481	0.487	0.470	0.511	0.748	0.923	0.970	0.932

Especially at lower frequencies, an important frequency dependence of C^{-2} vs V is quite clear. This can be explained by taking into account the series resistance of the device [18]. It can be seen that all of these plots are nearly linear. This indicates that the formation of these structures is resemble a Schottky diode and allows the use of the simple depletion layer theory (Eq. (9)) and the linearity in plot of C^{-2} vs V indicates that the charge density within the depletion region of the structure is uniform. Some parameters of the structure are listed in Table 1 by using the reverse bias *C–V* characteristics. As can be seen Table 1, the values of the diffusion potentials and Fermi energy levels are tend to increase towards to the high frequencies in the experimental errors.

The Schottky diode is electrically similar to a p–n junction, though the current flow in the diode is primarily due to majority carriers having an inherently fast response. It is used extensively for high-frequencies ($f \geq 500$ kHz). It is very often observed experimentally that the Schottky barrier height calculated from *I–V* characteristics is not equal the barrier height extracted from *C–V* measurements. This is observed especially at low frequencies (for *C–V* measurements) and non-ideal contacts. It is seen that the values of barrier heights higher than the value of the *I–V* measurements. In conclusion, the Schottky contacts are usually characterized by electrical techniques, most often by *I–V* or *C–V* measurements. Both techniques are differently sensitive to possible occurrence of inhomogeneities at the Schottky contact. As the current of the Schottky diode depends exponentially on the barrier height, inhomogeneities and especially small patches with a lower Schottky barrier height (SBH) at the contact, strongly influences the resulting apparent SBH. On the other hand, SBHs calculated from the *C–V* measurement have a tendency to be an average value of the SBHs of patches present in the contact (barrier height inhomogeneities that are present at the PPy/p-Si interface), that is, average barrier height is the mean value of the barrier minima plus barrier maxima. In most cases they are higher than the SBH extracted from *I–V* measurements [19]. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise, they will yield different values [24,25].

The capacitance–frequency (*C–f*) measurements of this structure was measured with an HP4192A LF capacitance-meter, at the various bias(0.00–0.26 V) with steps of 0.02 V. The junction capacitance is measured as a function of frequency and forward voltage.

The capacitance of the devices depending on frequency is given as: $C = C_{sc} + C_{ss}$ (at low frequency) and $C \cong C_{sc}$ (at high frequency), where C_{sc} is space charge capacitance, and C_{ss} is interface capacitance. The interface capacitance can be described as:

$$C_{ss} = AqN_{ss}\frac{\arctan(wt)}{w\tau} \tag{12}$$

where τ is the time constant and can be written as

$$\tau = \frac{1}{v_{th}\sigma N_A}\exp\left(\frac{qV_d}{kT}\right) \tag{13}$$

where σ is the cross section of interface states, v_{th} is the thermal velocity of the carrier, N_A is acceptor concentration, q is electron charge and k is Boltzmann constant. The interface state density for small values of $\omega\tau$ is equal to [21].

$$N_{ss} = \frac{C_{ss}}{qA} \tag{14}$$

where A is the diode area. The interface state capacitance (C_{sc}) is determined from the vertical axis intercept of *C–f* plots. In a p-type semiconductor, energy of the interface states E_{ss} with respect to the top of the valence band at the surface of semiconductor is described as [22]:

$$E_{ss} - E_v = q(\Phi_b - V) \tag{15}$$

where E_{ss} is the energy of interface states and E_v the valence band edge.

Fig. 6 shows *C–f* curves of PPy/p-Si Schottky diode at various bias voltages. Fig. 6 reveals that, the measured capacitance remained almost constant up to a certain value of the frequency at low frequencies. The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states in equilibrium with the p-Si that can follow the ac signal. As the frequency has increased further, the diode capacitance has first decreased sharply and then has decreased monotonically at high frequency as constant. Decreasing values of the capacitance in the intermediate frequency region mean that small part of the interface states can only follow the signal.

In addition, we fitted Eq. 25 in Ref. [23] (which agree with our explanations) to the experimental C_{ss} vs frequency at all biases to obtain the density of interface states and relaxation time. To obtain the dependence of density of interface states and relaxation time on bias, the fitting procedure was repeated for all values of bias. We found that the theoretical and experimental values had good agreement each other with at all biases. But, we show only one bias dependent plot. C_{ss} as a function of frequency at $V = 0.26$ V, both theoretical and

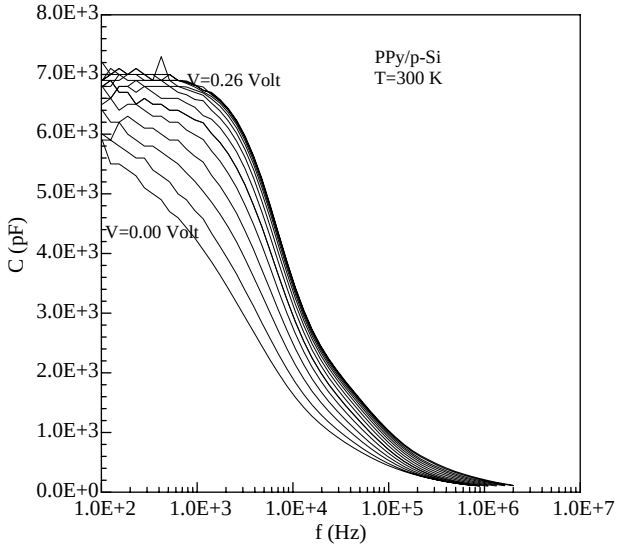

Fig. 6. The experimental *C–f* curves of the PPy/p-Si structure (0.00–0.26 V with steps of 0.02 V).

experimental, is shown in Fig. 7. Fig. 8 shows the experimental N_{ss} vs E_{ss}–E_v and τ vs E_{ss}–E_v plots, obtained from *C–f* characteristics. It is seen that while the interface states densities and the relaxation times show a decrease with bias from the top of the valance band towards the midgap slow, they decrease much more faster above the midgap towards the conduction band. As can be seen from Fig. 8, the interface state density N_{ss} obtained by the admittance spectroscopy method ranges from 9.80×10^{13} cm^{-2} eV^{-1} at 0.69 eV to 4.5×10^{15} cm^{-2} eV^{-1} at 0.43 eV. In addition, the values of the relaxation times range from 0.007 s at 0.69 eV to 0.089 s at 0.43 eV.

In conclusion, the study of some electrical properties of PPy/p-Si structure was investigated by using the *I–V, C–V* and *C–f* characteristics at room temperature in dark. The non-ideal forward bias *I–V* behaviour observed in the structure is attributed to a change in the polymer/semiconductor barrier height due to the interface states, the interfacial layer and series

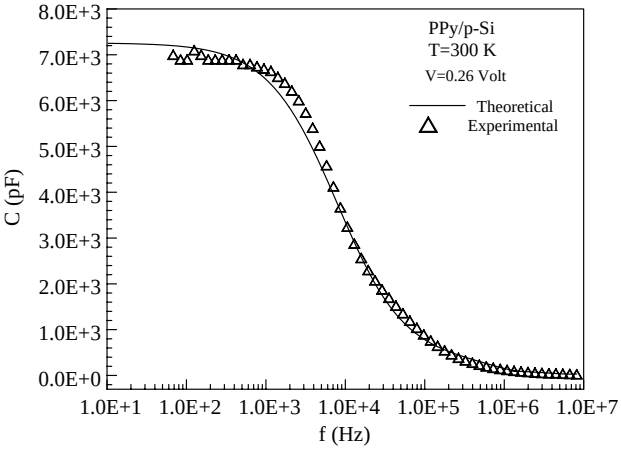

Fig. 7. Forward bias interface state capacitance plot as a function of frequency for a bias voltage of $V=0.04$ V both experimental and theoretical.

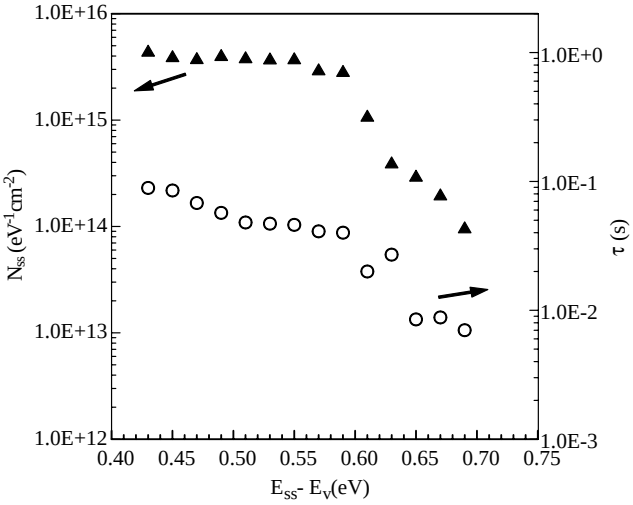

Fig. 8. The distribution plots of the interface state density and their time constant vs E_{ss}–E_v obtained from the *C–f* characteristics.

resistance. The values of ideality factor and the barrier height have been obtained from *I–V* characteristics as 1.78 and 0.69 eV, respectively. The downward curvature at sufficiently large voltages is caused by the effect of series resistance (R_s), apart from the presence of the interface states, which are in equilibrium with the semiconductor. The values of the R_s, the barrier height and the ideality factor have been calculated from the high voltage region of the structure (with Cheung functions) as $n=3.53$, $R_s=155\ \Omega$ by using Eq. (6) and by using Eq. (8) as $R_s=165\ \Omega$, $\Phi_b=0.64$ eV. The *C–V–f* measurements indicate that the capacitance measured varies with applied bias and frequency. In the low frequencies the reverse bias the value of capacitance is higher than the high frequencies. As can be seen Fig. 6, in the *C–f* characteristics, the measured capacitance remained almost constant up to a certain value of the frequency at low frequencies but it was decreased sharply towards high frequencies. The higher values of capacitance at low frequency attributed to the excess capacitance resulting from the interface states in equilibrium with the p-type Si that can follow the ac signal. The theoretical and experimental *C–f* characteristics of the structure were compared and it was seen that there was a good agreement between them. In summary this study, it can be said that this structure show good diode behaviour. According to the electrical characterization, in the future, it can be used rectifying contacts, integrated circuits, the other electronic devices and so on.

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